REMARKS

This Amendment is responsive to the final Office Action mailed on August 11, 2004. Claims 19 and 28-31 are amended herein. Claims 1-33 are pending.

Claims 28-33 are allowed. The Examiner has indicated that claims 13, 19 and 23-26 contain allowable subject matter.

The Examiner has objected to claim 19 due to the misspelling of the word "for" as "fir" in the claim. Claim 19 is amended herein to change "fir" to "for". Withdrawal of the objection to claim 19 is respectfully requested.

Claims 1-4, and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Peterson (U.S. 5,986,712) in view of Vetro (U.S. 6,490,320).

Claims 5-10 and 14-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Peterson in view of Vetro and further in view of Tabatabai (U.S. 5,686,964).

Claims 11-12, 18, and 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Peterson in view of Vetro and further in view of Ozkan (U.S. 5,838,686).

Applicants respectfully traverse these rejections.

Discussion of Amended Claims

Claim 19 is amended as discussed above to overcome the Examiner's objection thereto.

Allowed claims 28-31 were presented in Applicants' prior Amendment. Each of claims 28-31 are based on a combination of claim 1 with the allowable subject matter of the dependent claims 13, 19, 23, and 24, respectively (including the subject matter of intervening claims). These claims are amended herein to correct certain errors noted in the way in which these claims were combined in the prior Amendment. The amended claims 28-31 now more accurately reflect the original subject matter of the claims that were combined.

Discussion of the Prior Art

Peterson discloses an apparatus that maintains a bit budget for encoding video pictures. The bit budget of Peterson is used to manage the decoder VBV model so that the VBV does not overflow or underflow (Abstract, Col. 3, lines 25-43). In contrast, the present invention manages a budget of a number of processing cycles for a transcoder processor. A processor cycle budget as claimed by Applicants is very different from a bit budget as disclosed in Peterson. A processor cycle budget manages the amount of processing resources needed to perform a task. A bit budget manages the amount of bits allocated for encoding each portion of a picture.

Further, as acknowledged by the Examiner, Peterson does not disclose a transcoder processor which operates in a plurality of transcoding modes, as set forth in Applicants' claims 1 and 27.

Accordingly, Peterson does not disclose or remotely suggest:

- maintaining a budget of a number of processing cycles that are available at a transcoder processor to process video data;
- maintaining an estimate of the number of processing cycles required by the processor to process the video data;
- providing the video data to the processor;
- wherein the processor operates in a plurality of transcoding modes; and
- selecting one of the modes for processing each video frame according to a relationship between a number of budgeted processing cycles and an estimated number of required processing cycles.

In fact, Peterson does not even discuss processing modes of a processor, and therefore cannot be seen to disclose the subject matter of Applicants' claims as indicated by the Examiner.

Vetro fails to remedy the defects of Peterson. Vetro teaches content-based transcoding techniques for various levels of a video. The levels include a program level, a shot level, a frame level and video object level, and a sub-region level (Vetro et al. at col. 6, lines 1-10). Vetro discloses selecting transcoding modes based on network constraints. The network constraints,

such as channel bandwidth limitations, and are independent of processor cycles. Therefore, the mode selection of Vetro is independent of processor cycles.

Accordingly, Vetro does not disclose or suggest selecting a processing mode for each video frame according to a relationship between the number of budgeted processing cycles and the estimated number of required processing cycles, as claimed by Applicants.

Applicants' respectfully submit that combining the disclosures of Peterson and Vetro would not result in Applicants' claimed invention as apparently assumed by the Examiner, since the combination of Peterson and Vetro do not disclose or remotely suggest all the features of Applicants' independent claims 1 and 27 as discussed above.

With regard to Applicants' claim 3, the Examiner indicates that Peterson's computation of the nominal number of bits allocated to each stripe is equivalent to Applicants' claimed language "wherein the estimated number of required processing cycles is updated after each video frame is processed" set forth in claim 3. Applicants respectfully submit that the Examiner has misinterpreted either the disclosure of Peterson or Applicants' claim language.

Computing the number of bits used to encode a frame or picture as in Peterson is very different than computing the number of processing cycles of a processor. The number of bits generated and budgeted depends on the amount of video compression, complexity of the video content, size of video frames, and channel bandwidth. The number of processing cycles depends primarily on the method of transcoding used (e.g., transcode, re-quant, or bypass). The number of processing cycles also depends on input bitstream characteristics, such as the number of coefficients.

Accordingly, Peterson does not disclose or remotely suggest that an estimated number of required processing cycles is updated after each video frame is processed, as set forth in Applicants' claim 3.

The Examiner relies on a combination of the Peterson, Vetro and Tabatabai in rejecting claims 5-10 and 14-17. The Examiner has noted at page 4 of the Office Action that the Peterson in view of Vitro does not disclose requantization, full transcoding and bypass modes as claimed in claims 5 and 14-17. The Examiner relies on Tabatabai as disclosing the subject matter of

claims 5 and 14-17. Applicants' respectfully submit that Tabatabai does not cure the deficiencies of Peterson and Vetro.

Tabatabai merely discloses a bit rate control mechanism for video data compression that either estimates the number of bits required to represent a digital image or video at a particular quality in a compressed form or estimates the quality achievable for digital image or video when compressed to a given number of bits (Col. 1, lines 6-14). The Examiner has relied on Figure 3 of the Tabatabai reference as disclosing Applicants' claimed modes. Figure 3 is a simplified block diagram of an MPEG encoder used to control the quantity of data through compression. The Tabatabai mode selector is a MPEG-2 mode selector which selects between Intra coded blocks and motion estimated blocks, which are well known in the art as encoding modes. The upper switch of Figure 3 of Tabatabai is used for intra mode decisions. This is not bypass mode as claimed by Applicants, since the block input must go through the DCT and Quantization functions for processing. The lower switch of Figure 3 of Tabatabai uses motion estimation for Inter Coded blocks. There is no requantization in an MPEG-2 encoder and it is therefore not discussed in Tabatabai or Peterson. Vetro describes transcoding, but fails to teach or remotely suggest a requantization mode. Vetro does not refer to any mode selection. Thus, Tabatabai does not alone, or in combination with Peterson and Vetro, teach or suggest Applicants' invention as set forth in Claims 5 and 14-17.

The Examiner has also rejected claim 10 based on a combination of Peterson, Vetro, and Tabatabai. Applicants claim 10 specifies that the different processing modes have different computational intensities. As discussed above, the modes of Tabatabai are encoding modes, rather than processing modes as claimed by Applicants. Tabatabai does not disclose skipping of operations depending on mode selection and therefore the amount of computational intensity in Tabatabai is independent of processing mode selection (which as discussed above is also not disclosed in Tabatabai). Those skilled in the art would know that encoder mode selection, as disclosed in Tabatabai) is based on best video quality, and that computational intensity (as claimed by Applicants) depends on picture type (I, B, or P) and macroblock type (intra or inter).

Therefore, Tabatabai, in combination with Peterson and Vetro, fails to disclose or remotely suggest that different processing modes have different computational intensities, as set forth in Applicants' claim 10.

The Examiner has rejected claims 11-12, 18, and 20-22 in view of the combination of Peterson, Vetro, and Ozkan. Ozkan does not remedy the defects of the Peterson and Vetro. With regard to Applicant's claim 11, the Examiner is correct in indicating that Vetro teaches a plurality of channels. However, none of the references discloses separately maintaining a budget of a number of processing cycles and an estimated number of required processing cycles for each of the plurality of channels, as claimed by Applicants in claim 11. The Ozkan reference merely teaches a system for dynamically allocating a scarce resource among several competing users in response to indications of need from the users. The Ozkan reference is silent with respect to a transcoder processor to process video data. Ozkan and Peterson do not discuss processing cycles.

Further, Peterson does not disclose the determination of a processing cycle deficit as apparently assumed by the Examiner in rejecting claims 12, 18, and 20-22. The cited portion of Peterson relied on by the Examiner (Col. 5, lines 53-67 and Col. 6, lines 1-22) in rejecting claims 12, 18, and 20-22 refers only to a determination of whether the number of bits used by the encoder is greater than average or not. Peterson does not disclose any determination of a processing cycle deficit as claimed by Applicants.

In sum, the primary reference, Peterson, does not contain any discussion whatsoever of budgeted or estimated processing cycles, but rather only discusses determination of a bit budget to avoid a VBV buffer overflow. Applicants' respectfully submit that the Examiner's rejections are all based on a misunderstanding of the claimed invention and/or the disclosure of Peterson and as such should be withdrawn.

In view of the above, Applicants respectfully submit that the claimed invention would not have been obvious to one skilled in the art in view of the combination of Peterson and Vetro, taken alone or in combination with any of the other references of record.

Further remarks regarding the asserted relationship between Applicants' claims and the prior art are not deemed necessary, in view of the above discussion. Applicants' silence as to any of the Examiner's comments is not indicative of acquiescence to the stated grounds of rejection.

Conclusion

In view of the above, the Examiner is respectfully requested to reconsider this application, allow each of the presently pending claims, and to pass this application on to an early issue. If there are any remaining issues that need to be addressed in order to place this application into condition for allowance, the Examiner is requested to telephone Applicants' undersigned attorney.

Respectfully submitted,

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